

Aries PCIe[®]/CXL[®] Smart DSP Retimers

Benefits and Features

- 64/32/16/8/5/2.5 GT/s per lane with automatic link equalization
- Low latency for Compute Express Link[®] applications
- 8 and 16 Lanes with flexible link bifurcation
- Extends reach by 36 dB at 64 GT/s enabling low-cost PCB materials and connectors
- Integrated AC-coupling capacitors reduce solution footprint and improves signal integrity performance
- COnnectivity System Management and Optimization Software (COSMOS) suite for extensive Link, Fleet and RAS Management comes integrated with C and Python SDKs for rapid integration and customization of advanced in-band and out-of-band diagnostics
- Host management/diagnostics through fast I2C/I3C
- Firmware load through SPI Flash or EEPROM
- Seamless HW & SW upgradability across the portfolio utilizing industry standard footprints and COSMOS

Applications

- GPU/AI Accelerator data ingest and clustering
- General purpose server CPU connectivity for network, storage (SSD), accelerator, CXL memory, etc.
- PCIe riser and add-in cards for disaggregated compute, network, memory & storage connectivity

Description

Aries PCIe/CXL Smart DSP Retimers include three generations of protocol-aware, low-latency Retimers designed to integrate seamlessly between a root complex and endpoint(s), extending the reach by 3x. Compliant to all PCIe 6.x/5.0/4.0/3.0/2.0/1.0 rates and Retimer functional requirements, the Aries Smart Retimer enables more system topologies and lower total solution cost while minimizing implementation overhead and Bill of Materials (BOM).

To support a wide variety of endpoints and port configurations, the Aries x16 Smart Retimer can bifurcate to one x16 / two x8 / four x4 / eight x2 links and other combinations; the Aries x8 Smart Retimer can bifurcate to one x8 / two x4 / four x2 links and more. Each link operates independently, and per-link diagnostics information such as link state history and electrical margin are accessible through the COSMOS suite.

The pinout is based on the Intel Retimer Supplemental Specification and the device uses a Flip-Chip CSP package. The pinout allows for separate single-layer routing for all high-speed transmit and receive signals. Compact design, minimal supporting circuitry, and integrated AC-coupling capacitors reduces overall solution size, making the Aries Smart Retimer ideal for space-restricted applications like system boards and riser cards.

Part #	Retimer Gen	PCIe/CXL	Lanes	Status	Compatibility
PT6**2LR	3 rd	PCle 6.x	8,16	Sampling	- Seamless HW & SW - upgradability utilizing industry standard footprints and - COSMOS
PT6**2LX	3 rd	PCIe 6.x/CXL 3.x	8,16	Sampling	
PT5**2LR	3 rd	PCle 5.0	8,16	Sampling	
PT5**2LX	3 rd	PCIe 5.0/CXL 2.0	8,16	Sampling	
PT5**1LR	2 nd	PCIe 5.0	8,16	Production	
PT5**1LX	2 nd	PCIe 5.0/CXL 2.0	8,16	Production	
PT4***LR	1 st	PCle 4.0	8,16	Production	

Product Family Information

Astera Labs, Inc. reserves the right to update this brief without notice. For detailed information on specific products, please refer to the data sheet.



AI Server Platform Application

The Aries PCIe[®]/CXL[®] Smart DSP Retimer portfolio provides robust PCIe connectivity in AI server platforms with complex topologies, densely packed signals that travel longer distances, and an increasing number of connectors that are utilized to expand configuration optionality.



Astera Labs' Intelligent Connectivity Platform

The Aries PCIe[®]/CXL[®] Smart DSP Retimer portfolio is an integral part of Astera Labs' Intelligent Connectivity Platform. In addition to Aries, there are multiple PCIe, CXL and Ethernet ICs, Modules & Boards that are at the foundation of the platform. Astera Labs' COnnectivity System Management and Optimization Software (COSMOS) suite provides extensive Link, Fleet and RAS Management features and diagnostics. Through the combination of software and hardware, the Intelligent Connectivity Platform enables a smart connectivity backbone that is both scalable and customizable for AI and cloud infrastructure.



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