www.AsteraLabs.com

Position: **Senior Package & Platform Engineer**

Location: San Francisco Bay Area

Overview:
Astera Labs Inc., a leader in purpose-built connectivity solutions for data-centric systems, is seeking a **Senior Package and Platform Engineer** in Santa Clara, CA with experience supporting development of semiconductor products for high-speed communications protocols like PCIe, Ethernet, Infiniband, DDR, NVMe, USB, etc.

Job Description:
As an Astera Labs Senior Package and Platform Engineer, you will be part of a team that designs-in and supports Astera Labs' portfolio of connectivity products in the world's leading cloud service providers and server and networking OEMs. In this role, you will need to execute on package engineering deliverables during development, qualification, initial ramp, and high-volume production.

Basic qualifications:
- Strong academic/technical background in electrical engineering; Bachelor's is required; Master's preferred.
- Minimum of 5 years of experience working in a role that includes hands-on elements of semiconductor package development including BOM definition, Flip-chip package technology, design constraints and package netlist generation.
- Proven track record defining package BOM that enable device features creating value for customers. Understanding of package technologies, working with leading OSATs through the design manufacturing, qualification and release to production.
- Cross-functional design mentality working with silicon design community to develop optimized chip-package architecture that enable customers' features (PCI-Express, Ethernet, DDR4/5, Power delivery).
- Professional attitude, hands-on work ethic with the ability to prioritize a dynamic list of multiple tasks, working closely with the design, applications and quality engineers working with minimal guidance and supervision to deliver a quality solution.
- Authorized to work in the US and start immediately.

Required experience:
- Package design flow experience using Cadence and/or Mentor Graphics toolset. Able to produce package netlists defining the chip to package interconnect including passive components.
- Strong signal integrity skills working with high speed SERDES protocols (PCI-Express, Ethernet, DDR4/5) and the ability to optimize high speed package traces based on simulation and extraction of nets. Knowledge using high speed design tools such as ADS & HFSS a strong desire.
- Power integrity skills with knowledge to optimize on-package capacitors to meet IP constraints.
- Experience bringing new package BOMs into NPI leveraging existing technologies and using industry standard qualification processes.
- Quality mindset putting the silicon health at the center of all development activities.
- Hands-on knowledge of NRZ/PAM4 SerDes protocols like PCIe, Ethernet (25G and above), etc. and/or memory interfaces such as (LP)DDR5/4/3.
- Proven track record of implementing Electrical and package level reliability tests, including HAST, HTOL, ESD, Temperature cycle, dynamic warpage.