www.AsteraLabs.com

Position: **Senior Product Engineer**

Location: San Francisco Bay Area

Overview:
Astera Labs Inc., a leader in purpose-built connectivity solutions for data-centric systems, is seeking a **Senior Product Engineer** in Santa Clara, CA with experience supporting development of semiconductor products for high-speed communications protocols like PCIe, Ethernet, Infiniband, DDR, NVMe, USB, etc.

Job Description:
As an Astera Labs Senior Product Engineer, you will be part of a team that designs-in and supports Astera Labs' portfolio of connectivity products in the world's leading cloud service providers and server and networking OEMs. In this role, you will need to execute on product engineering deliverables during development, qualification, initial ramp, and high volume production.

Basic qualifications:
- Strong academic/technical background in electrical engineering; Bachelor's is required; Master's preferred.
- Minimum of 5 years of experience working in a role that includes hands-on elements of semiconductor development, characterization, and release to production.
- Proven track record creating characterization plans, characterization programs and working with the greater engineering community to obtain and analyze data across silicon, voltage and temperature corners.
- Professional attitude with the ability to prioritize a dynamic list of multiple tasks, working closely with the design, applications and ATE engineers working with minimal guidance and supervision to deliver a quality solution.
- Authorized to work in the US and start immediately.

Required experience:
- Working knowledge using ATE platforms, program flow and test optimization, Advantest V93000 strongly preferred.
- Experience leveraging OSAT partnership to develop execution plan for characterization, ATE development and production rollout.
- Quality mindset putting the silicon health at the center of all development activities.
- Strong analysis skills for architecting the scope of silicon characterization, obtaining the results and determining datasheet limits.
- Hands-on knowledge of NRZ/PAM4 SerDes protocols like PCIe, Ethernet (25G and above), etc. and/or memory interfaces such as (LP)DDR5/4/3.
- Demonstrated knowledge of common SerDes equalization circuits such as CTLE, DFE, FFE, and DSP.
- Proven track record of implementing Electrical and package level reliability tests, including HAST, HTOL, ESD, Temperature cycle, dynamic warpage.
- Experience using and automating lab equipment (protocol analyzers and high-speed oscilloscopes).
- Familiarity with high-speed and high power board design techniques.

Preferred experience:
- Working with silicon validation teams to ensure device performance meets production requirements.
- Firmware development in C/C++, scripting in Python, or other equivalent programming experience.