Astera Labs Cloud-Scale Interop Lab

PCIe Smart Retimers Test Report

Test Date	30-Mar-2021
Test Operator	Jonathan Bender

DEVICE UNDER TEST

System Element	Manufacturer	Model #	Serial #	FW #	Description
Endpoint	ACME	XYZ123	abc000000	1.0.0	Gen4 x4 U.2 SSD

ASTERA LABS DEVICE

System Element	Manufacturer	Model #	Silicon Revision	FW #	Description
Retimer	Astera Labs	PT4161L	A0	1.0.24	Gen4 x16 Retimer

RESULTS SUMMARY

Test Section	Description	Results	Comment
1	Intel PCIe Loop Tests	PASS	
2	AMD System Deck	PASS	
3	Intel RX Margining	PASS	
	Overall Result	PASS	

TEST 1

Platform Name	Manufacturer	BIOS Version	Root Complex	Tool	Tool Version	Special Hardware
Wilson City (#x)	Intel	16.D10	Ice Lake	PCIe Loop Test	xxx.xxx.xxx	The PT4161L is mounted on an Astera SVB (add-in card), and the DUT is plugged into an OCulink adapter connected to the SVB's CEM connector.

Test #	Description	Iterations	Other Args	Max Rate / Width	Result	Comment
1.0	testType=0: Secondary Bus Reset	1000	socket=0, port=9	Gen4 x4	PASS	
1.1	testType=1: Basic Link Retrain	1000	socket=0, port=9	Gen4 x4	PASS	
1.2	testType=2: Link Disable	1000	socket=0, port=9	Gen4 x4	PASS	
1.3	testType=3: D3hot (PM L1)	1000	socket=0, port=9	Gen4 x4	PASS	
1.4	testType=4: TxEq Retrain	1000	socket=0, port=9	Gen4 x4	PASS	
1.5	testType=5: Speed Change (all)	1000	socket=0, port=9	Gen4 x4	PASS	Gen 1 -> 2 -> 3 -> 4 -> 1 …
1.6	testType=6: Speed change (min/max)	1000	socket=0, port=9	Gen4 x4	PASS	Gen 1 -> 4 -> 1 …
1.7	Power Cycle Test 1: Cold Boot (AC)	10		Gen4 x4	PASS	
1.8	Hot Unplug / Plug test	10	socket=0, port=13	Gen4 x4	PASS	
1.9	Power Cycle Test 2: Warm Reboot	10		Gen4 x4	PASS	

Notes

1. Astera Labs defines a Intel PCIe Loop test to pass if no uncorrectable errors, speed errors, or width errors are reported by the tool during the course of testing.

TEST 2

Platform Name	Manufacturer	BIOS Version	Root Complex	Tool	Tool Version	Special Hardware
ROMED8-2T/ ETHANOL	AMD	1.00/RXM1000C	EPYC 7252/ MILAN ES100	System Deck	1.01.00.00	The PT4161L is mounted on an Astera SVB (add-in card), and the DUT is plugged into the Astera SVB's CEM connector.

Test #	Description	Iterations	Other Args	Max Rate / Width	Result	Comment
2.0	Secondary Bus Reset	1000		Gen4 x4	PASS	
2.1	Link Disable	1000		Gen4 x4	PASS	
2.2	Speed Change (all)	1000		Gen4 x4	PASS	Gen 1 -> 2 -> 3 -> 4 -> 1 …
2.3	Power Cycle Test: Cold Boot (AC)	10		Gen4 x4	PASS	

Notes

1. Astera Labs defines a System Deck test to pass if no Link Errors are reported by the tool during the course of testing, and the link maintains its maximum advertised speed and width.

TEST 3

Platform Name	Manufacturer	BIOS Version	Root Complex	Tool	Tool Version	Special Hardware
Wilson City (#x)	Intel	16.D10	Ice Lake	Intel PCIe Lane Margining Tool	1.2	The PT4161L is mounted on an Astera SVB (add-in card), and the DUT is plugged into an OCulink adapter connected to the SVB's CEM connector.

Test #	Description	Timing (L, R)	Voltage (Up, Dn)	Max Rate / Width	Result	Comment
3.0	Receiver 3, Lane 0:3 (min)	(-20%, 34.3%)	(119mV, -104mV)	Gen4 x4	PASS	Min value per result across all lanes
3.1	Receiver 3, Lane 0:3 (max)	(-31.4%, 40%)	(152mV, -148mV)	Gen4 x4	PASS	Max value per result across all lanes
3.2	Receiver 3, Lane 0:3 (avg)	(-25.7%, 38%)	(131mV, -124mV)	Gen4 x4	PASS	Average of each result