www.AsteraLabs.com
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Suite 204
Santa Clara, CA 95054

Senior Design Verification Engineer (Multiple Openings)

With a moderate degree of independent decision-making capability and moderate supervision, the Senior Design Verification Engineer will be responsible for System on a Chip (SoC) design verification, defining a chip verification plan, validating protocol performance, building and verifying environments, scripts, and tests for Astera Labs proprietary semiconductor connectivity technology. Duties include:

- Defining a comprehensive design verification methodology for a complex SoC which can ensure that the product will comply to a variety of industry standards (PCIe, I2C, Ethernet, etc.) and meet numerous customer-specific requirements;
- Developing an SoC verification environment based on Universal Verification Methodology (UVM) principles to enable functional verification and formal verification of SoC designs;
- Creating, reviewing, and implementing test plans, test cases, and test procedures to ensure complete functional and non-functional test coverage for high-speed communication protocols and associated verification IPs (VIPs);
- Running tests and regression simulations, reviewing results, and identifying root cause for any/all failing cases using Synopsys VCS simulator;
- Implementing necessary changes in the register transfer language (RTL) design based on simulation results and root cause analysis.

This position requires a bachelor's or foreign equivalent in EE, CE, or closely related field and five (5) years progressive professional experience as a Design/Verification Egr; Staff Egr, or closely related occupation.

Must have professional experience with:

- UVM (Universal Verification Methodology);
- High Speed DDR Interface (DDR4);
- PCI-Express;
- Verilog;
- System Verilog;
- Object Oriented Programming (C/C++).