www.AsteraLabs.com
2901 Tasman Dr.,
Suite 204
Santa Clara, CA 95054

Principal Electronic Engineer (Physical Design) (Multiple Openings)

With a high degree of independent decision-making capability and minimum supervision, the principal electronic engineer (physical design) will be responsible for all aspects of System On a Chip (SOC) physical design and implementation for astera labs proprietary semiconductor connectivity technology. Duties include:

- Defining a comprehensive physical design methodology for a complex SOC which can ensure successful integration of various ip blocks;
- Developing custom SOC design scripts needed for integrating various ip blocks, converting verilog code to gate-level netlist, inserting design for test (dft) components into the design, place and route, timing closure, and layout versus schematic (LVS) and design rule check (DRC) verification, etc.;
- Synthesizing custom verilog code into gate-level netlist and inserting dft components;
- Implementing synthesized into physical design by using advanced place-and-route tools, running timing analysis reports and iterating on the design to meet timing goals;
- Using advanced voltage drop analysis tools to ensure adequate power delivery and robust electromigration across the design;
- Completing physical verification (LVS and DRC) and formal verification to ensure physical design matches rtl description and passes all foundry mandated checks; and
- Working with the foundry to ship the physical design (GDS) to start wafer level manufacturing.

This position requires a bachelor's or foreign equivalent in EE, CE, or closely related field and five (5) years progressive professional experience as a Design Engineer; ASIC Engineer; Hardwre Engineer, or closely related occupation.

Must have professional experience with:

- Synthesis: Design Complier;
- Place and Route: IC Compiler II, IC Compiler;
- Noise Analysis AND Signal Integrity Analysis: Primetime-SI;
- Power Analysis (EM AND IR DROP ANALYSIS): Apache Redhawk;
- Scripting Languages: TCL, PERL and UNIX;
- Parasitic Extraction (RC Extraction): Starrc, Starrc-XT;
- Static Timing Analysis: Primetime;
- Formal Verification:, LEC, Formality;
- Physical Verification (DRC/LVS/ANT): ICV