

Principal Design Verification Engineer (Multiple Openings)

With a high degree of independent decision-making capability and minimum supervision, the Principal Design Verification Engineer will be responsible for architecting System on a Chip (SoC) design verification and overseeing chip verification environment, tests and implementation and defining protocol performance for Astera Labs' proprietary semiconductor connectivity technology. Duties include:

- Architecting a comprehensive design verification methodology for a complex SoC which can ensure that the product will comply to a variety of industry standards (PCIe, I2C, Ethernet, etc.) and meet numerous customer-specific requirements;
- Overseeing the development of SoC verification environment based on Universal Verification Methodology (UVM) principles to enable functional verification and formal verification of SoC designs;
- Defining test plans, test cases, and test procedures to ensure complete functional and non-functional test coverage for high-speed communication protocols and associated verification IPs (VIPs);
- Overseeing the running tests and regression simulations, reviewing results, and identifying root cause for any/all failing cases using Synopsys VCS simulator;
- Overseeing the implementation of necessary changes in the register transfer language (RTL) design based on simulation results and root cause analysis.

This position requires a master's or foreign equivalent in EE, CE, or closely related field and three (3) years experience as a Design/Verification Engineer; Staff Engineer, or closely related occupation.

* Will also accept Bachelors degree in EE, CE or closely related field + 5 years of progressive experience as Design/Verification Engineer; Staff Engineer or closely related occupation.*

Must have professional experience with:

- UVM (Universal Verification Methodology);
- High speed DDR interface (PCIe, DDR4, LPDDR4);
- Verilog HDL;
- System Verilog tests, and assertions;
- Object oriented programming (C/C++/Python)