Aries PCI Express® 4.0 and 5.0 Smart Retimers System Validation Board (SVB)

1 Introduction

The Astera Labs Aries System Validation Board (ARIES-X16-SVB-REVB), is intended for in-system evaluation of the Aries PCIe Gen-4/Gen-5 x16 Retimer. It has a x16 PCIe CEM-compliant edge finger to be plugged into a Gen-4/Gen-5 system and features a x16 CEM connector on top to install an endpoint add-in card. It is configured for plug-and-play operation, meaning no device configuration is required and the Root Complex (e.g. CPU) and Endpoint (e.g. NIC) will automatically form a Link through the Aries Retimer on power-up and de-assertion of PERST#. A Python SDK is available to read out various diagnostics information gathered by the Aries Retimer through the I2C interface to a PC. In addition to the required power regulators and pin-strap passives, the SVB has a number of additional debug features accessible through the Python SDK and I2C bus that allow for scripted read/write of all GPIOs, voltage and power information, temperature, separate reference clock path, and more.

Contact info@AsteraLabs.com for the SVB User's Guide and SDK.

Figure 1: ARIES-X16-SVB-REVB top side