www.AsteraLabs.com

Title: **Test Engineer, Astera Labs, Santa Clara, CA**

Astera Labs Inc., a leader in purpose-built connectivity solutions for data-centric systems, is looking for senior/principal **Test Engineers** for their Santa Clara (California) Design Center. Partnering with leading processor vendors, cloud service providers, seasoned investors and world-class manufacturing companies, Astera Labs is helping data-centric system designers remove performance bottlenecks in compute-intensive workloads such as Artificial Intelligence and Machine Learning. For more information about Astera Labs, see www.AsteraLabs.com.

We are looking for senior/principal **Test Engineers** with proven experience in developing and supporting complex mixed-signal silicon SoC products. The ideal candidate will develop and oversee SoC test strategy, interact with manufacturing partners, write and implement ATE programs and own the product from design, initial samples all the way through high volume production ramp. The candidate should have working knowledge of communication/interface protocols such as PCI-Express (Gen-4/5), Ethernet, Infiniband, DDR, NVMe, USB, etc.

Basic qualifications:

- Strong academic and technical background in electrical engineering. At minimum, a Bachelor's in EE is required, and a Master's is preferred.
- ≥8-year experience releasing complex SoC/silicon products to high volume manufacturing.
- Working knowledge of high-speed protocols like PCIe, Ethernet, Infiniband, DDR, NVMe, USB, etc.
- Professional attitude with ability to execute on multiple tasks with minimal supervision.
- Strong team player with good communication skills to work alongside a team of high caliber engineers.
- Entrepreneurial, open-mind behavior and can-do attitude.

Required experience:

- Hands-on experience with high speed mixed-signal SoC test program/hardware development on multiple high-speed test platforms.
- Collaboration with design team to define test strategy, create and own test plan.
- Tester platform selection, design and development of ATE hardware for wafer sort and final test.
- Familiar with high speed load board design techniques.
- Proven track record of implementing ATE patterns to optimize tester resources and minimize ATE test time while maintaining product quality.
- Strong knowledge and development of DFT techniques implemented in silicon that provide maximum defect and parametric device coverage – SCAN, MEMBIST, SerDes and other functional tests.
- Skilled in control interfaces – I2C, I3C, SPI, MDIO, JTAG etc.
- Expertise in production test of high speed SerDes operating at 16Gbps and higher.
- Skilled in ATE programming, silicon/ATE bring-up, bench-ATE correlation and debug.
- Experience with lab equipment including protocol analyzers and oscilloscopes.

Preferred experience:

- Fluent in data processing using high level programming languages.
- Familiarity with modern databases.