www.AsteraLabs.com

Title: **Principal/Senior Digital Design Engineer, Astera Labs, Santa Clara, USA.**

Astera Labs Inc., a leader in purpose-built connectivity solutions for data-centric systems, is seeking senior/principal **Digital Design Engineers** for their Santa Clara (California) Design Center. Partnering with leading processor vendors, cloud service providers, seasoned investors and world-class manufacturing companies, Astera Labs is helping data-centric system designers remove performance bottlenecks in compute-intensive workloads such as Artificial Intelligence and Machine Learning. For more information about Astera Labs, see www.AsteraLabs.com.

We are looking for senior/principal **Digital Design Engineers** with experience developing micro-architecture and implementation of the front-end circuit design, including RTL, synthesis, IP integration, and block-level verification for high performance network controllers. The candidate must have good knowledge of communication/interface protocols such as PCI-Express (Gen-3 and above), Ethernet, Infiniband, DDR, NVMe, USB, etc.

Basic qualifications:

- Strong academic and technical background in electrical engineering. A Bachelor's degree in EE is required, and a Master's degree is preferred.
- ≥8 years' experience supporting or developing complex SoC/silicon products for Server, Storage, and/or Networking applications.
- Professional attitude with the ability to prioritize a dynamic list of multiple tasks, plan and prepare for customer meetings in advance, and work with minimal guidance and supervision.
- Entrepreneurial, open-mind behavior and can-do attitude. Think and act fast with the customer in mind!
- Authorized to work in the US and start immediately.

Required experience:

- Hands-on, thorough knowledge of high-speed protocols like PCIe, Ethernet, Infiniband, DDR, NVMe, USB, etc.
- Proven front end design expertise – architecture, RTL, simulations, synthesis, timing closure, GLS, DFT etc.
- Full chip or block level ownership from architecture to GDS, driving multiple complex designs to production
- Experience with Cadence and/or Synopsys digital design tools/flows
- Good knowledge of design for test (DFT), stuck-at and transition scan test insertion
- Familiarity with UVM based design verification
- Silicon bring-up and debug expertise
- Small-geometry CMOS (≤28nm) design

Preferred experience:

- Firmware development with C-language, scripting with Python or other equivalent programming languages.
- Development/support for PCIe or Ethernet Switch products.