www.AsteraLabs.com

Title: **Principal/Senior Design Verification Engineer, Astera Labs, Santa Clara, USA.**

Astera Labs Inc., a leader in purpose-built connectivity solutions for data-centric systems, is seeking senior/principal **Design Verification Engineers** for their Santa Clara (California) Design Center. Partnering with leading processor vendors, cloud service providers, seasoned investors and world-class manufacturing companies, Astera Labs is helping data-centric system designers remove performance bottlenecks in compute-intensive workloads such as Artificial Intelligence and Machine Learning. For more information about Astera Labs, see www.AsteraLabs.com.

We are looking for senior/principal **Design Verification Engineers** with proven experience in all aspects of verification in UVM from start to finish. The candidate must have experience using Verification IPs from 3rd party vendors and a good knowledge of communication protocols such as PCI-Express (Gen-3 and above), Ethernet, Infiniband, DDR, NVMe, USB, etc.

Basic qualifications:

- Strong academic and technical background in electrical engineering. At minimum, a Bachelor's in EE is required, and a Maser's is preferred.
- ≥8 years' experience supporting or developing complex SoC/silicon products for Server, Storage, and/or Networking applications.
- Professional attitude with the ability to prioritize a dynamic list of multiple tasks, to plan and prepare for customer meetings in advance, and to work with minimal guidance and supervision.
- Entrepreneurial, open-mind behavior and can-do attitude. Think and act fast with the customer in mind!
- Authorized to work in the US and start immediately.

Required experience:

- Hands-on in UVM, strong knowledge on UVM constructs (uvm_callback, uvm_sequence, uvm phases)
- Must be able to work independently to develop test-plans, and related test-sequences exercising the right stimuli and work collaboratively with RTL designers to debug failures.
- Develop user-controlled random constraints in transaction-based verification methodology. Experience writing assertions, cover properties.
- Must have prior experience using Verification IPs from 3rd party vendors for communication protocols such as PCI-Express (Gen-3 and above), Ethernet, Infiniband, DDR, NVMe, USB, etc.
- Integrate Verification IPs to core design and build env layer on top of it.
- Strong familiarity with generating coverage using VCS, analyzing Coverage Data using tools like Synopsys DVE/Verdi.
- Understanding of management buses like I2C/JTAG.
- Working knowledge of running gate level simulation and SDF back annotation

Preferred experience:

- RTL design expertise is a plus, including asynchronous clock domain crossing and FIFO verification
- Physical Layer, Link Layer and Transaction Layer verification expertise in PCIe protocol
- Experience with FPGA-based verification/emulation